

REMARKS

This response is a full and complete response to the Office Action, dated December 24, 2009. In the present Office Action, the Examiner has noted that claims 1-21 are pending, that claims 1-7 and 9-21 stand rejected under 35 U.S.C. §102(b) as anticipated by Henrion (U.S. Patent 5,461,615), and that claim 8 is objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Assignee has amended claims 1, 2, 5, 8, and 10 without prejudice. Support for claim amendments may be found in the Specification at least at FIG. 4 and page 8, line 9 through page 9, line 28, for example. Accordingly, such amendments include no new matter.

In view of both the amendments presented above and the following remarks, it is submitted that the claims pending in the application are novel and nonobvious. It is believed that this application is in condition for allowance. By this response, reconsideration of the present application is respectfully requested.

Allowable Subject Matter

Assignee thanks the Examiner for noting allowability of claim 8. However, Assignee points out that this claim merely sets forth examples of allowable subject matter and that other claims supported by the disclosure of this application are also allowable.

Assignee has amended claims 1, 2, 5, 8, and 10 without prejudice; however, it is noted that these amendments do not narrow claim scope and, rather, in most cases, broaden claim scope. Therefore, no prosecution history estoppels results from the foregoing amendments.

35 U.S.C. § 102(b) Rejection

Claims 1-7 and 9-21 stand rejected under 35 U.S.C. §102(b) as anticipated by Henrion (U.S. Patent 5,461,615). This rejection is respectfully traversed.

To anticipate a claim under §102, a document must show how each and every element of the claim. “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” [MPEP §2131.01] Henrion does not teach each and every element of the rejected claims.

In rejecting claim 1, the Examiner asserts that Henrion discloses a method for assigning an address to a node in a network having an arbitrary topology, including providing a first address to a first node such that the first address includes a description of a path to the first node, and establishing a mapping between a plurality of output ports in the network and bits in the first address such that a packet, directed to the first address node, at a second node in the network is forwarded via an output port on the second node in the network, in response to a specified bit in the first address having a specified value.

However, Assignee asserts that Henrion fails to disclose a method to assign self-routing addresses for packets as recited in claim 1, for example. In particular, Henrion's nodes (switching elements) in the switching network (such as SN1 in FIG. 2) apparently route packets (cells) according to binary numbers in sets of bits of internal routing labels (col. 8, lines 29-35). Therefore, Henrion does not teach or show forwarding a packet to an output port in response to a specified value of a specified bit of the internal routing label. Therefore, since Henrion does not teach or suggest each and every limitation of claim 1, assignee requests withdrawal of the rejection of this claim under 35 USC 102(b).

While differing in scope from claim 1 at least in part, claims 9, 11, 15, and 19 recite similar limitations to claim 1. Assignee respectfully submits that these claims, and claims 2-7, 10, 11-14, 16-18, and 20, depending therefrom, therefore similarly distinguish over Henrion. Accordingly, Assignee respectfully requests withdrawal of the rejection of claims 9, 11, 15, and 19 and their dependent claims 2-7, 10, 11-14, 16-18, and 20 under 35 U.S.C. § 102(b).

Assignee further submits that Henrion has not established a mapping between the output ports of network nodes (switching elements) and bits on the internal routing label. For example, Henrion describes in col. 8, lines 12-15 that “The internal routing label constituted by an output address OPA then includes a plurality of sets of bits each identifying one output of a switching element through which the cell must pass.” From col. 8, lines 18-35, a binary number is apparently used in each set of bits of the internal routing label to identify the node (switching

element) output, e.g., 111 for the 8-th output of the node, for example. However, Assignee submits that there is no mapping between the output ports of nodes and bits on the internal routing label.

Assignee also respectfully disagrees with the Examiner's assertion that "irregular groups of outputs" in Henrion (col. 9, lines 26) is equal to "a network having an arbitrary topology," as set forth in claim 1.

It is noted that claimed subject matter may be patentably distinguished from the applied document for several reasons, including those discussed above; the foregoing is believed to be sufficient to overcome the Examiner's rejections, although additional reasons are also available.

Further, it is noted that the Assignee's failure to comment directly upon any of the positions asserted by the Examiner in the office action does not indicate agreement or acquiescence with those asserted positions since the Examiner's other positions are believed to be moot in light of the foregoing. Accordingly, the Assignee reserves the right to pursue un-amended claims in a continuing application.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all the claims pending in this patent application are in condition for allowance. Reconsideration and allowance of all the claims are respectfully solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Brian D. Wichner at (503) 439-6500 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

In the event there are any errors with respect to the fees for this response or any other papers related to this response, the Director is hereby given permission to charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account No. 50-3130.

Respectfully submitted,

By /Brian D. Wichner, Reg. No. 52,359/
Brian D. Wichner, Patent Agent
Registration No. 52,359

Dated: March 3, 2010

Customer No. 43831
Berkeley Law and Technology Group, LLP
17933 NW Evergreen Parkway, Suite 250
Beaverton, OR 97006
Phone: 503.439.6500
Fax: 503.439.6558